Abstract

[0055] A method for modeling a memory with delay back annotation in accordance with the VITAL application specific integrated circuit modeling specification begins with modeling the memory with a timing generic and a port declaration. The wire delay of the memory is then modeled, followed by modeling a timing check for the memory. The wire delay of the model of the memory is then created. A description of the functional operation of the memory is then generated. The path delay for the address, control, and data bus signals to the memory is formed by overloading the VITAL path delay procedures. The VITAL timing check procedures are overloaded to determine timing constraint violations of the timing bus signals of the memory. The VITAL wire delay procedures are overloaded to determine interconnection delay bus signals of the memory.